Dmux\_1x4\_4bit: PASS

Crossbar\_2x2\_4bit: PASS

Crossbar\_4x4\_4bit: PASS

Toggle\_Flip\_Flop: PASS

Crossbar\_2x2\_4bit:

- Using in[3:0] to connect to a single AND gate implies performing an AND operation on all 4 bits of 'in'. It's better to represent this with four individual AND gates in gate-level design.

- Testbench design needs to consider more possible cases.

- No explanation for the testbench design.

Crossbar\_4x4\_4bit:

- Try covering all the combinations of inputs in your testbench.

- Please explain how the circuit works and why can it realize target function with more detail.

- You didn't list the unachievable output combinations.

FPGA:

Take Away Part:

- It is great that you have learned how to perform gate-level design using Verilog. You can continue practicing to further develop your skills. I believe that you will do well.

- You can share more about what you have learned from this lab to make it more comprehensive.